PRELIMINARY

CY7C1061G/CY7C1061GE

16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
  - t_{AA} = 10 ns/15 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
  - I_{CC} = 90-mA typical at 100 MHz
  - I_{SB2} = 20-mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

Functional Description

CY7C1061G and CY7C1061GE are high-performance CMOS fast static RAM devices with embedded ECC[1]. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY7C1061GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable ($\overline{CE}$) input LOW. To access dual chip enable devices, assert both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High and Byte Low Enable ($\overline{BHE}$, $\overline{BLE}$) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH for a single chip enable device and $\overline{CE}_1$ HIGH / CE_2 LOW for a dual chip enable device), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

On the CY7C1061GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the Truth Table on page 16 for a complete description of read and write modes.

The logic block diagrams are on page 2.

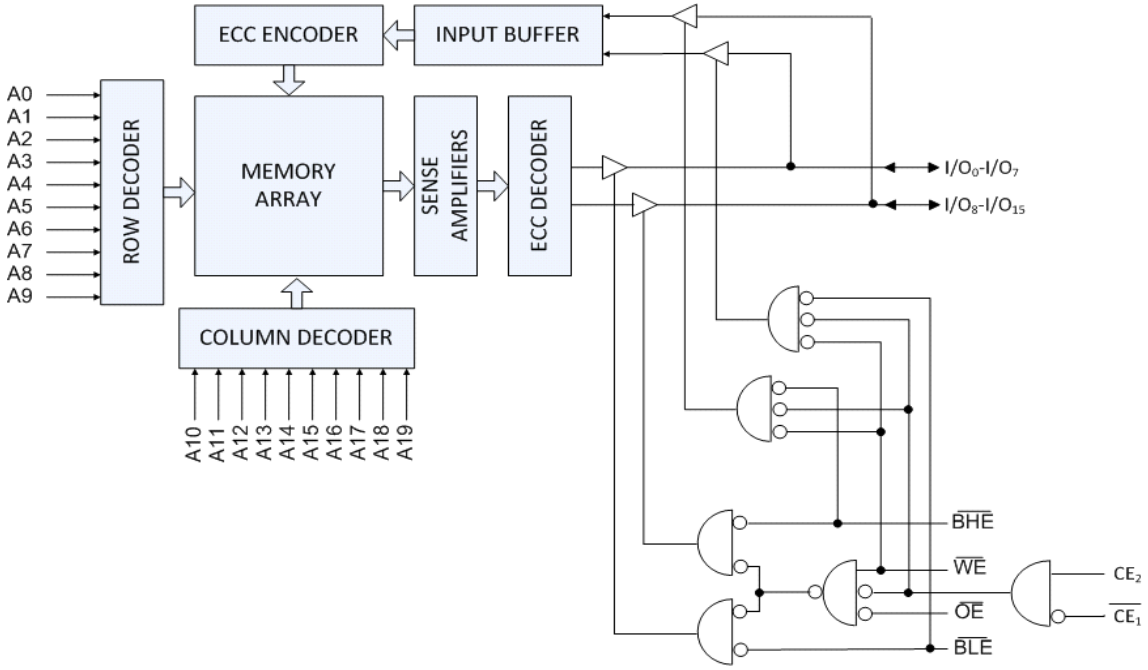
The CY7C1061G and CY7C1061GE devices are available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

Product Portfolio

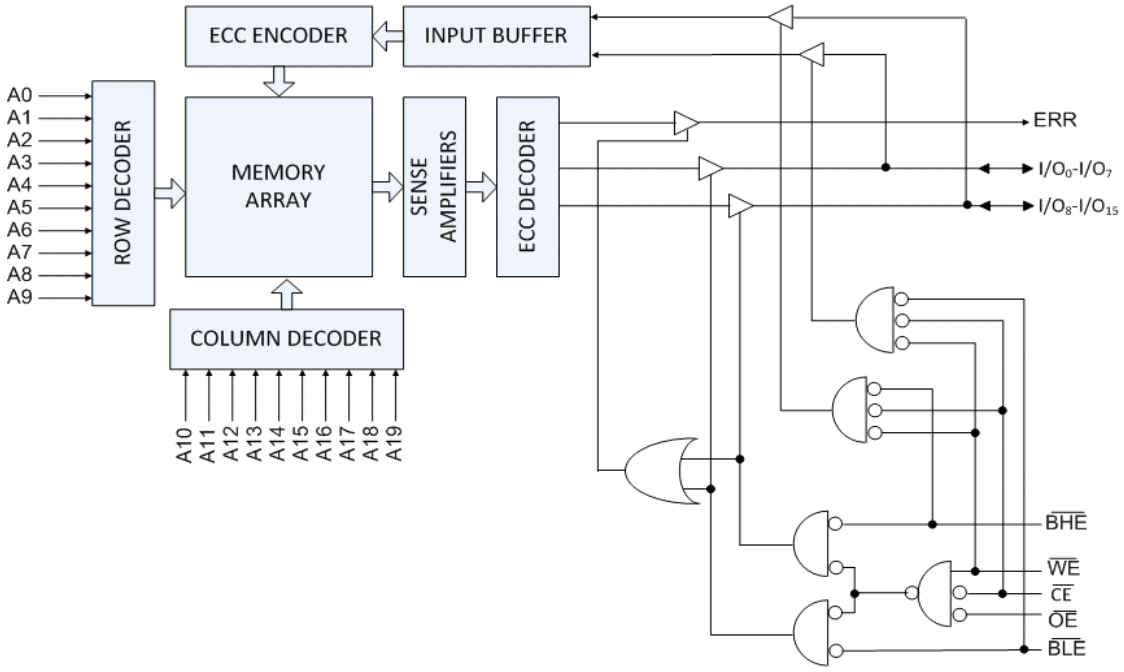
Product	Features and Options (see the Pin Configurations section)	Range	V_{CC} Range (V)	Speed (ns) 10/15	Current Consumption			
					Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
					Typ[2]	Max	Typ[2]	Max
CY7C1061G18	Single or dual chip enables	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1061G(E)30			2.2 V–3.6 V	10	90	110		
CY7C1061G	Optional ERR pins Address MSB A_{19} pin placement options compatible with Cypress and other vendors		4.5 V–5.5 V	10	90	110		

Notes
1. This device does not support automatic write-back on error detection.
2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1061G



Logic Block Diagram – CY7C1061GE



Contents

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Dual Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G[3] Package/Grade ID: BVJXI

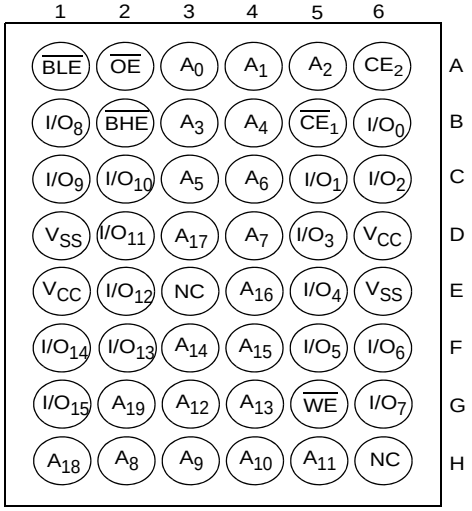


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Dual Chip Enable without ERR, Address MSB A19 at Ball H6, CY7C1061G[3] Package/Grade ID: BVXI

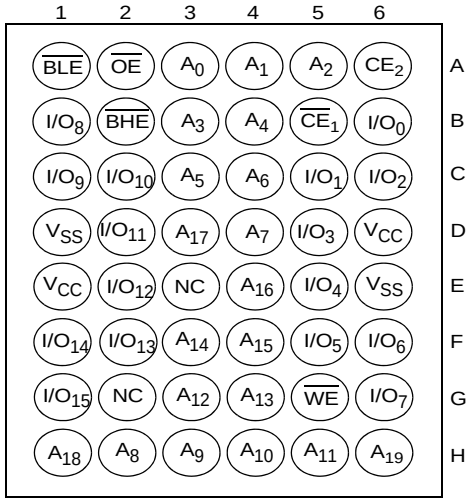
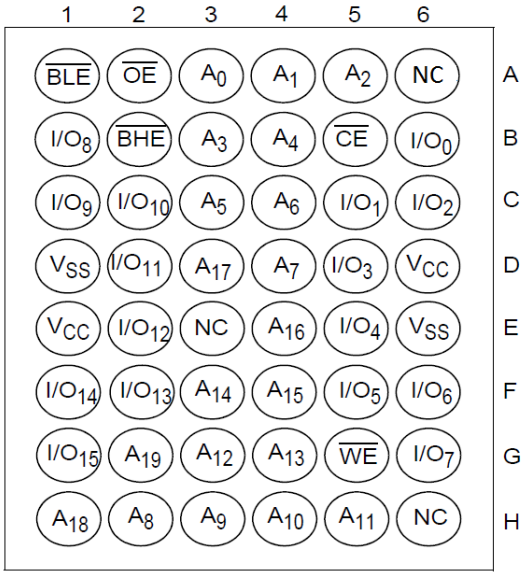


Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G[3] Package/Grade ID: BV1XI



Note
3. NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm)
Single Chip Enable with ERR, Address MSB A19 at Ball G2
CY7C1061GE[4, 5] Package/Grade ID: BV1XI

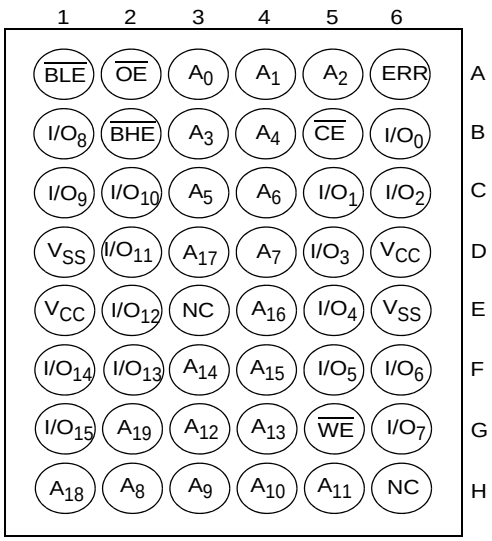


Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm)
Dual Chip Enable with ERR, Address MSB A19 at Ball G2
CY7C1061GE[4, 5] Package/Grade ID: BVJXI

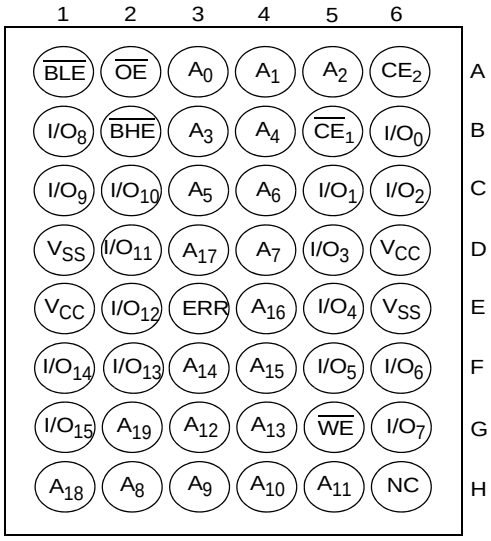
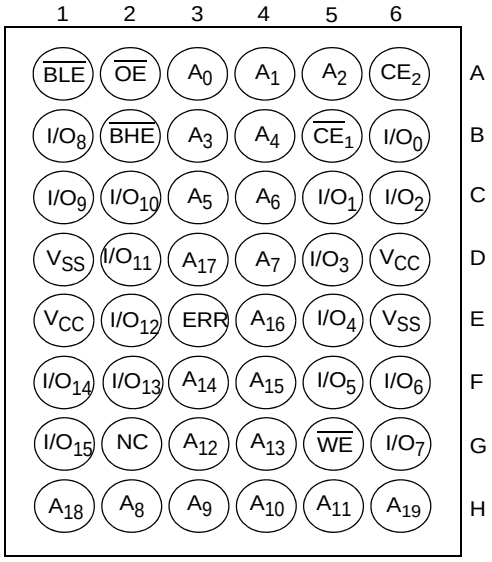


Figure 6. 48-ball VFBGA (6 × 8 × 1.0 mm) Dual Chip Enable with ERR, Address MSB A19 at Ball H6
CY7C1061GE[4, 5] Package/Grade ID: BVXI



Notes
4. NC pins are not connected internally to the die.
5. ERR is an output pin.

Pin Configurations (continued)

Figure 7. 48-pin TSOP I (12 × 18.4 × 1 mm) Single Chip Enable with ERR CY7C1061GE[6, 7] Package/Grade ID: ZXI

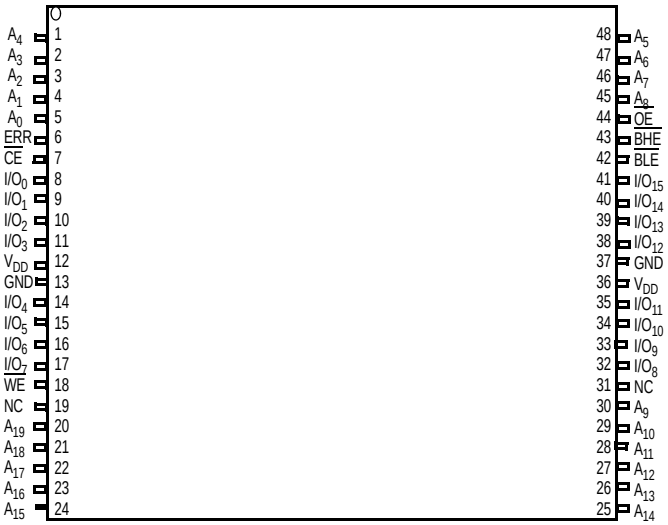


Figure 8. 48-pin TSOP I (12 × 18.4 × 1 mm) Single Chip Enable without ERR CY7C1061G[6] Package/Grade ID: ZXI

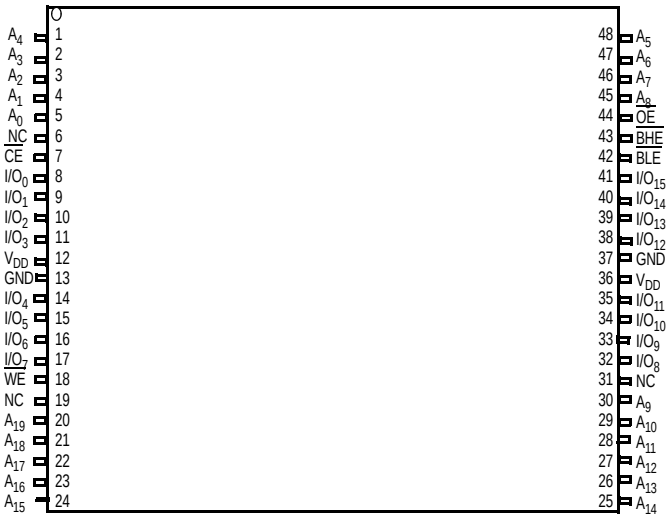


Figure 9. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Dual Chip Enable without ERR CY7C1061G[6] Package/Grade ID: ZSXI

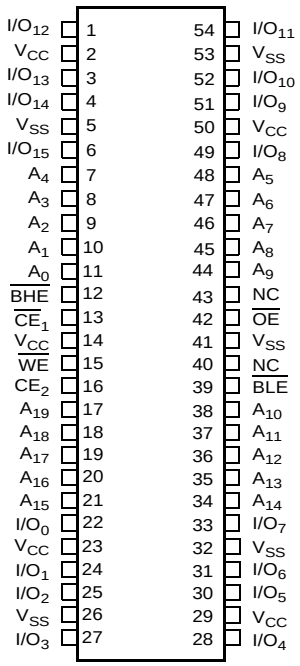
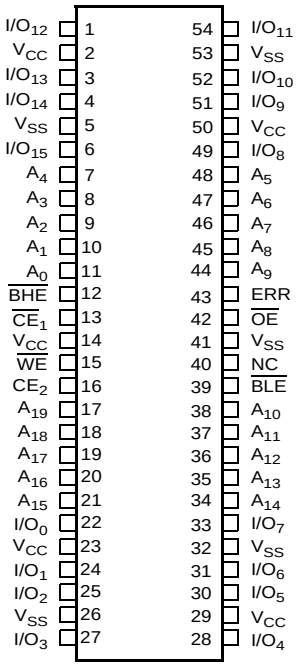


Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Dual Chip Enable with ERR CY7C1061GE[6, 7] Package/Grade ID: ZSXI



Notes
6. NC pins are not connected internally to the die.
7. ERR is an output pin.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND .....–0.5 V to +6.0 V

DC voltage applied to outputs in High Z State [8] .....–0.5 V to V_{CC} + 0.5 V

DC input voltage[8] .....–0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions		10 ns / 15 ns			Unit
					Min	Typ[10]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.0	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}[8]	Input HIGH voltage	1.65 V to 2.2 V			1.4	–	V_{CC} + 0.2	V
		2.2 V to 2.7 V			2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V			2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V			2.2	–	V_{CC} + 0.5	
V_{IL}[8]	Input LOW voltage	1.65 V to 2.2 V			–0.2	–	0.4	V
		2.2 V to 2.7 V			–0.3	–	0.6	
		2.7 V to 3.6 V			–0.3	–	0.8	
		4.5 V to 5.5 V			–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	µA
I_{CC}	Operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	110.0	mA
				f = 66.7 MHz	–	70.0	80.0	
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH} [9], V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	40.0	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V[9], V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0	30.0	mA

Notes

8. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.
9. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
10. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Capacitance

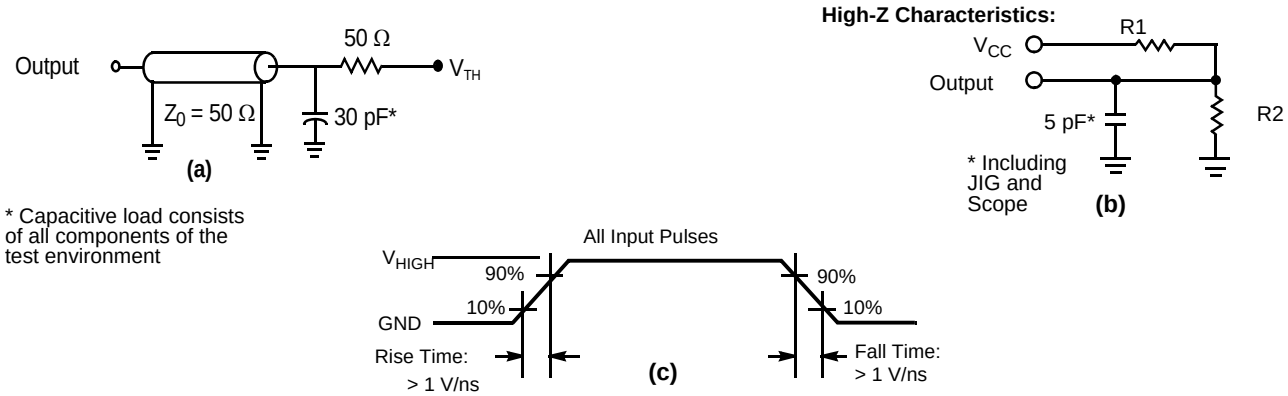
Parameter [11]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	10	10	pF
C_{OUT}	I/O capacitance		10	10	10	pF

Thermal Resistance

Parameter [11]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		21.58	15.75	13.42	°C/W

AC Test Loads and Waveforms

Figure 11. AC Test Loads and Waveforms[12]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full-device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 100-µs wait time after V_{CC} stabilizes to its operational value.

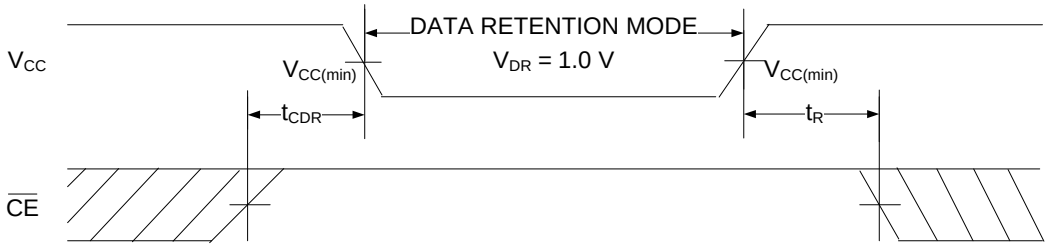
Data Retention Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V[13], $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30.0	mA
t_{CDR}[14]	Chip deselect to data retention time		0	–	ns
t_R[15]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	ns
		$V_{CC} < 2.2$ V	15.0	–	ns

Data Retention Waveform

Figure 12. Data Retention Waveform[13]



Notes

13. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full-device operation requires linear V_{CC} ramp from V_{DR} to V_{CC} (min) ≥ 100 µs or stable at V_{CC} (min) ≥ 100 µs.

AC Switching Characteristics

Over the operating range of –40 °C to 85 °C

Parameter [16]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{POWER}	V_{CC} (stable) to the first access[17]	100.0	–	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	15.0	–	ns
t_{AA}	Address to data / ERR valid	–	10.0	–	15.0	ns
t_{OHA}	Data / ERR hold from address change	3.0	–	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data / ERR valid [18]	–	10.0	–	15.0	ns
t_{DOE}	$\overline{OE}$ LOW to data / ERR valid	–	5.0	–	8.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low-Z [19, 20]	0	–	1.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high-Z [19, 20]	–	5.0	–	8.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low-Z [18, 19, 20]	3.0	–	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high-Z [18, 19, 20]	–	5.0	–	8.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up [18, 21]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [18, 21]	–	10.0	–	15.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	–	8.0	ns
t_{LZBE}	Byte enable to low-Z [19,20]	0	–	1.0	–	ns
t_{HZBE}	Byte disable to high-Z [19,20]	–	6.0	–	8.0	ns
Write Cycle [22, 23]						
t_{WC}	Write cycle time	10.0	–	15.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end[18]	7.0	–	12.0	–	ns
t_{AW}	Address setup to write end	7.0	–	12.0	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	12.0	–	ns
t_{SD}	Data setup to write end	5.0	–	8.0	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low-Z [19, 20]	3.0	–	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high-Z [19, 20]	–	5.0	–	8.0	ns
t_{BW}	Byte Enable to write end	7.0	–	12.0	–	ns

Notes

16. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading, shown in part (a) of Figure 11 on page 8, unless specified otherwise.
17. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed
18. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
19. t_{HZOE}, t_{HZCE}, t_{HZWE}, and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 11 on page 8. Hi-Z, Lo-Z transition is measured ±200 mV from steady state voltage.
20. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
21. These parameters are guaranteed by design and are not tested.
22. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 13. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled)[24, 25]

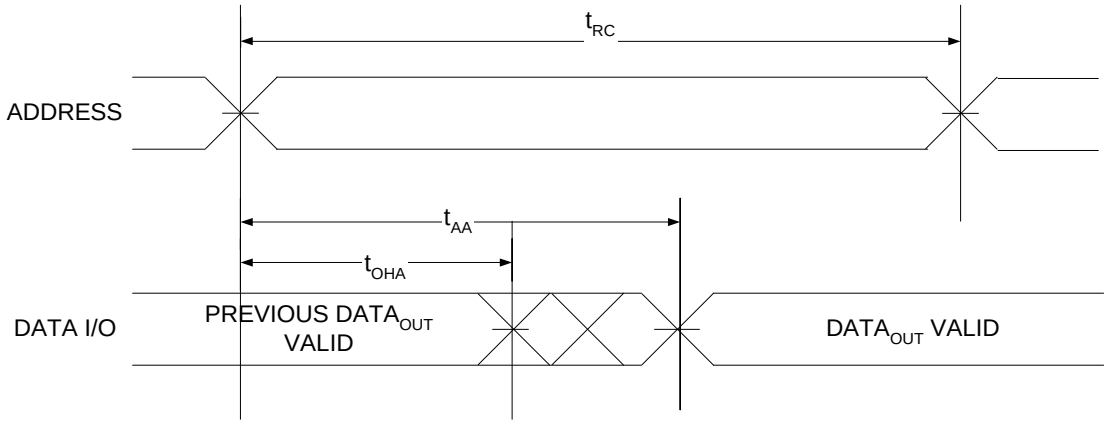
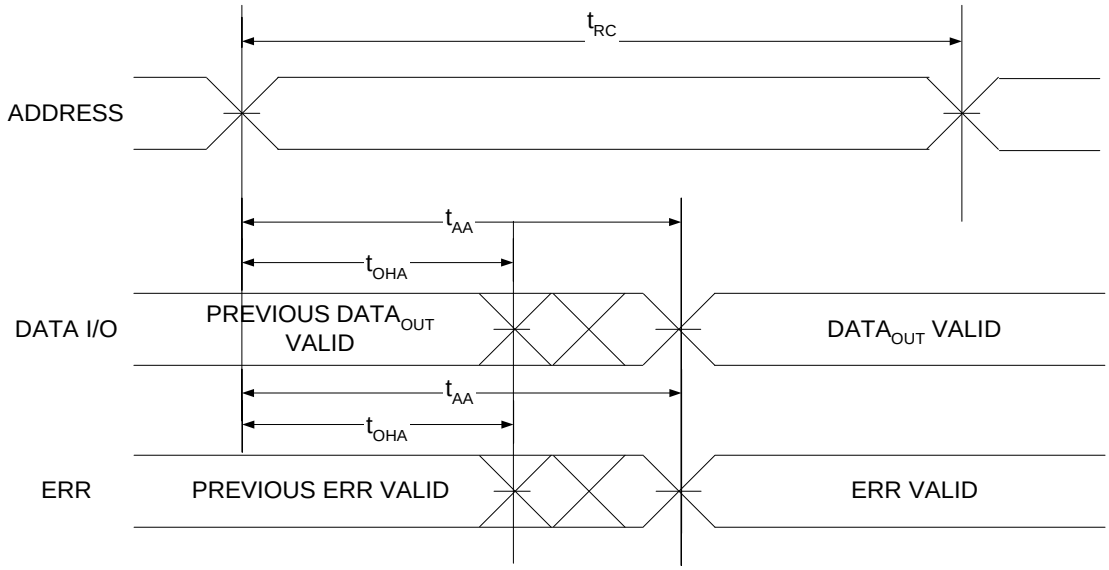


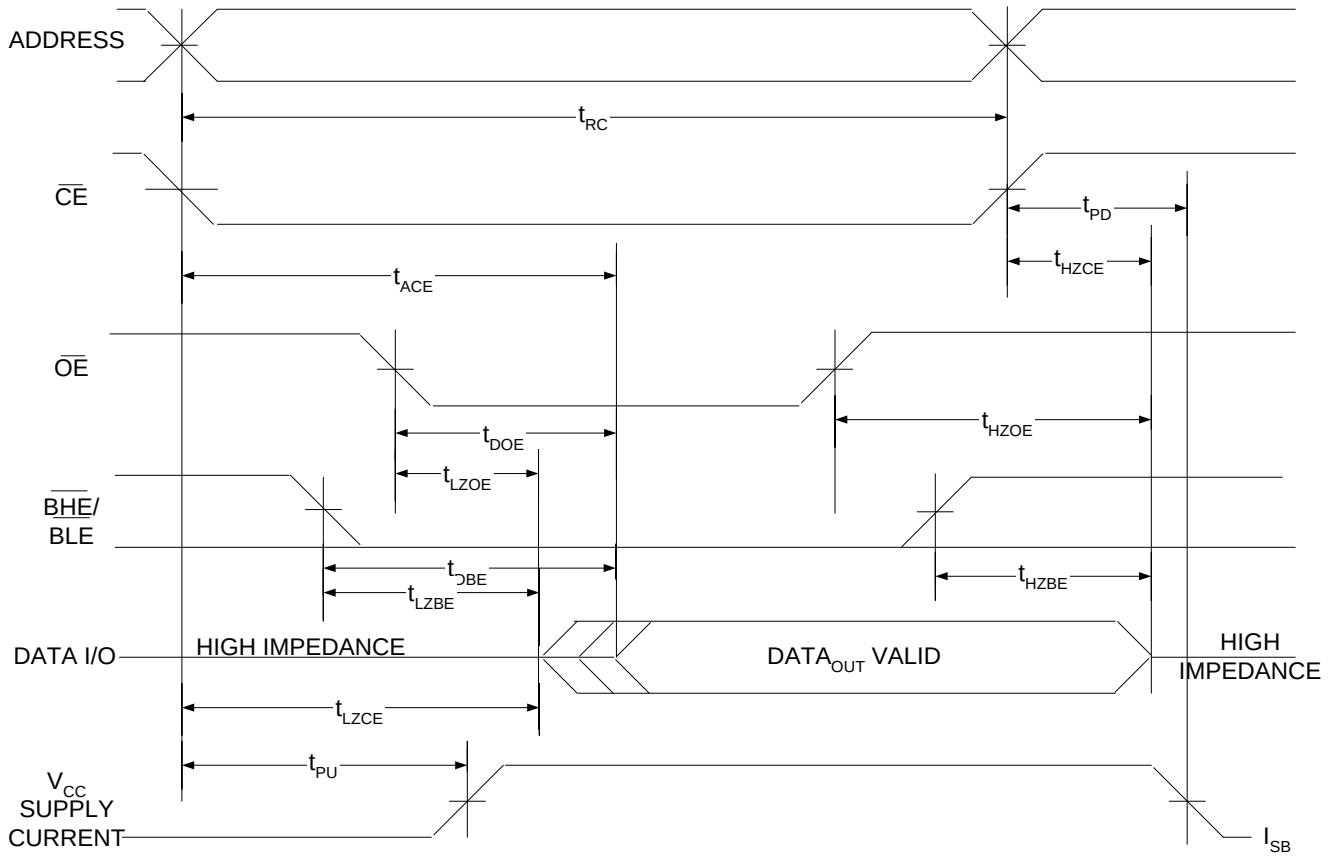
Figure 14. Read Cycle No. 2 of CY7C1061GE (Address Transition Controlled)[24, 25]



Notes
24. The device is continuously selected, $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
25. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 15. Read Cycle No. 3 ($\overline{OE}$ Controlled)[26, 27, 28]



Notes

26. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
27. $\overline{WE}$ is HIGH for read cycle.
28. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 16. Write Cycle No. 1 ($\overline{CE}$ Controlled)[29, 30, 31]

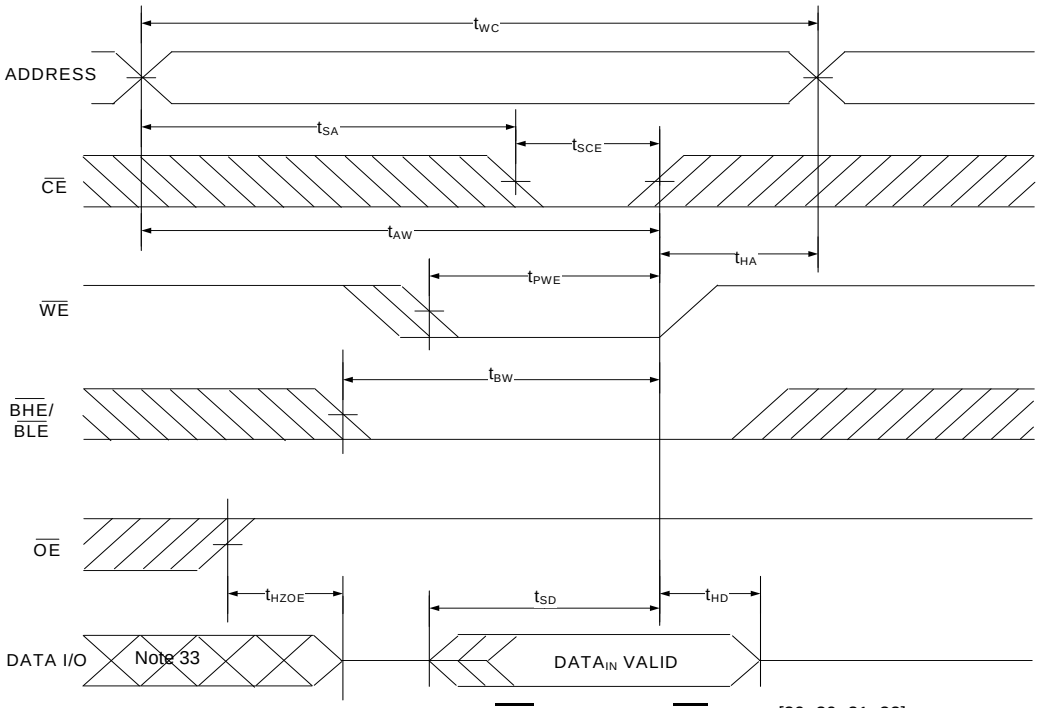
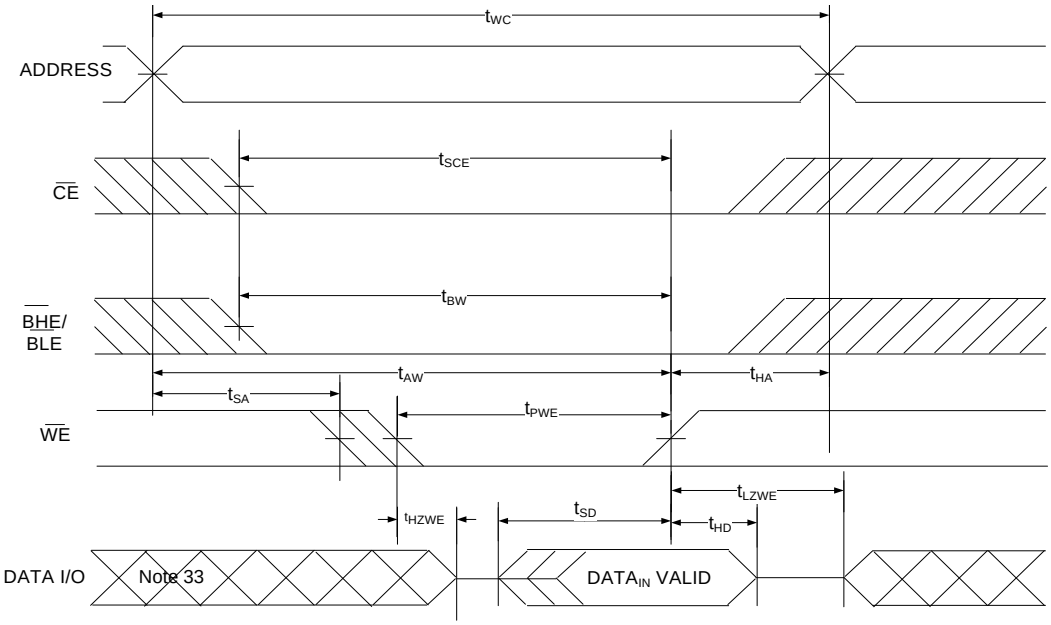


Figure 17. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[29, 30, 31, 32]

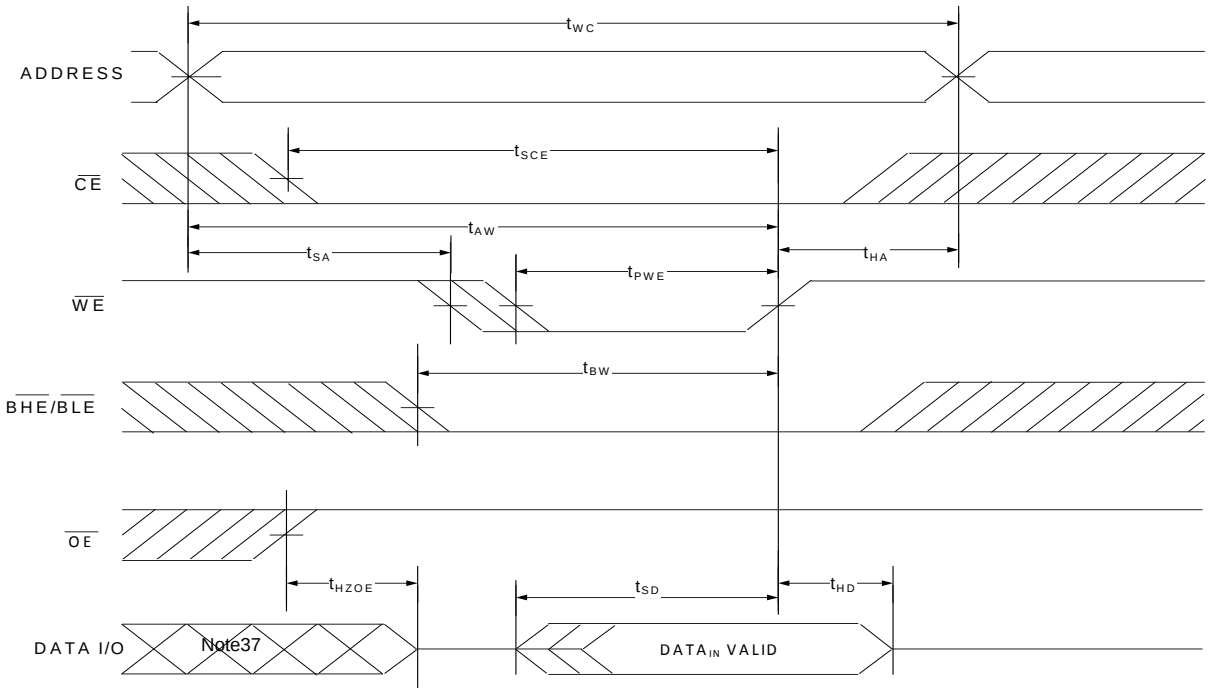


Notes

29. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
30. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
31. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
32. The minimum write cycle pulse width should be equal to sum of t_{HZWE} and t_{SD}.
33. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 18. Write Cycle No. 3 ($\overline{WE}$ controlled)[34, 35, 36]

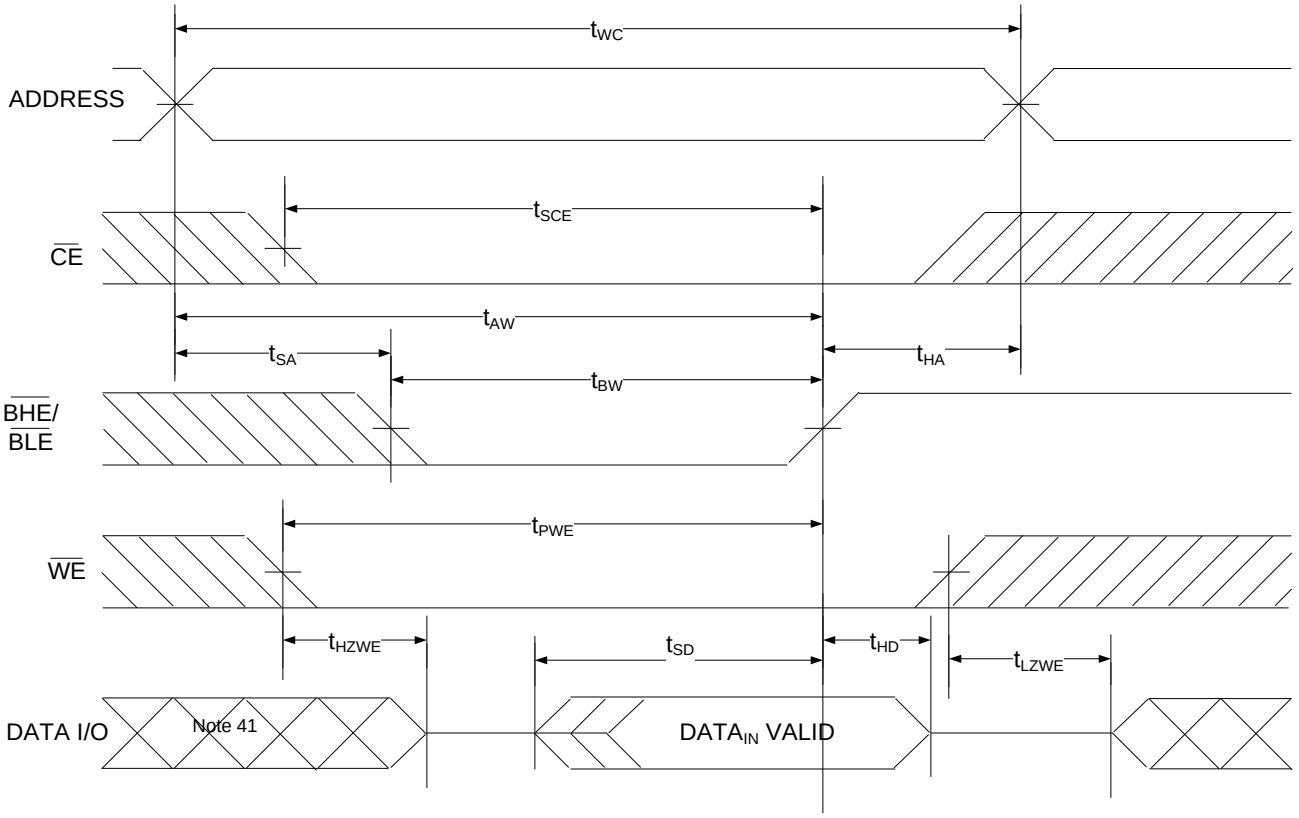


Notes

34. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
35. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
36. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
37. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 19. Write Cycle No. 4 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)[38, 39, 40]



Notes

38. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
39. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
40. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
41. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [42]	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X[43]	X[43]	X[43]	X[43]	High-Z	High-Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7C1061GE

Output	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected or outputs disabled or Write operation

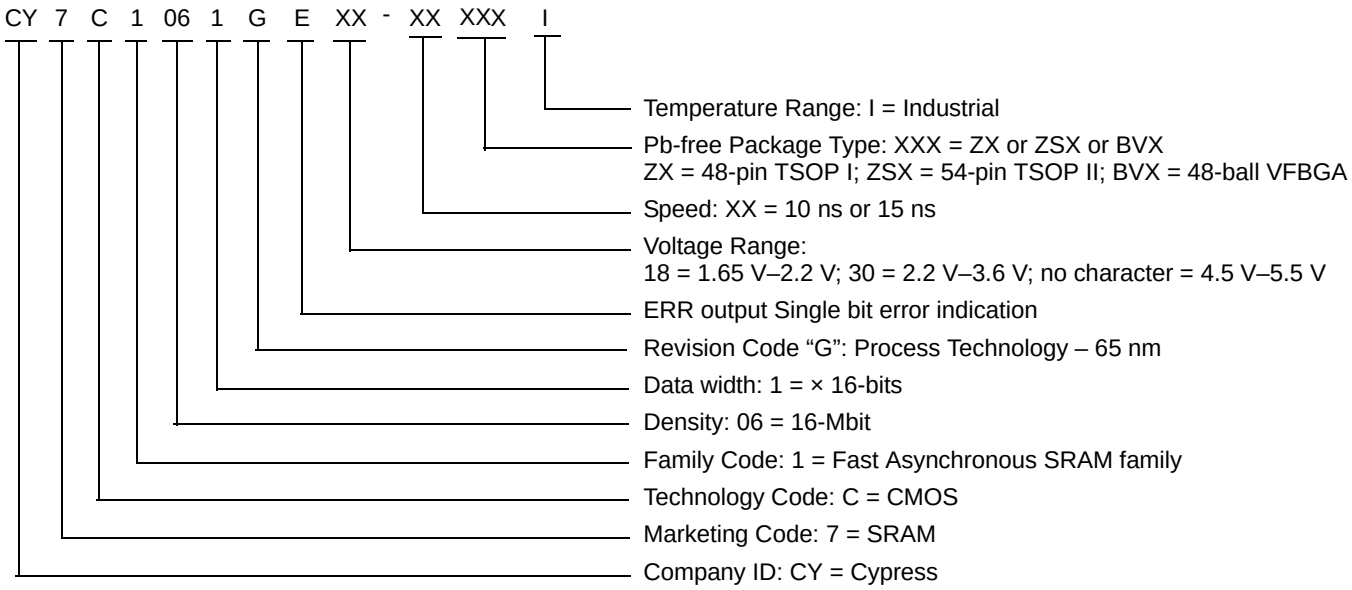
Notes

42. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
43. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

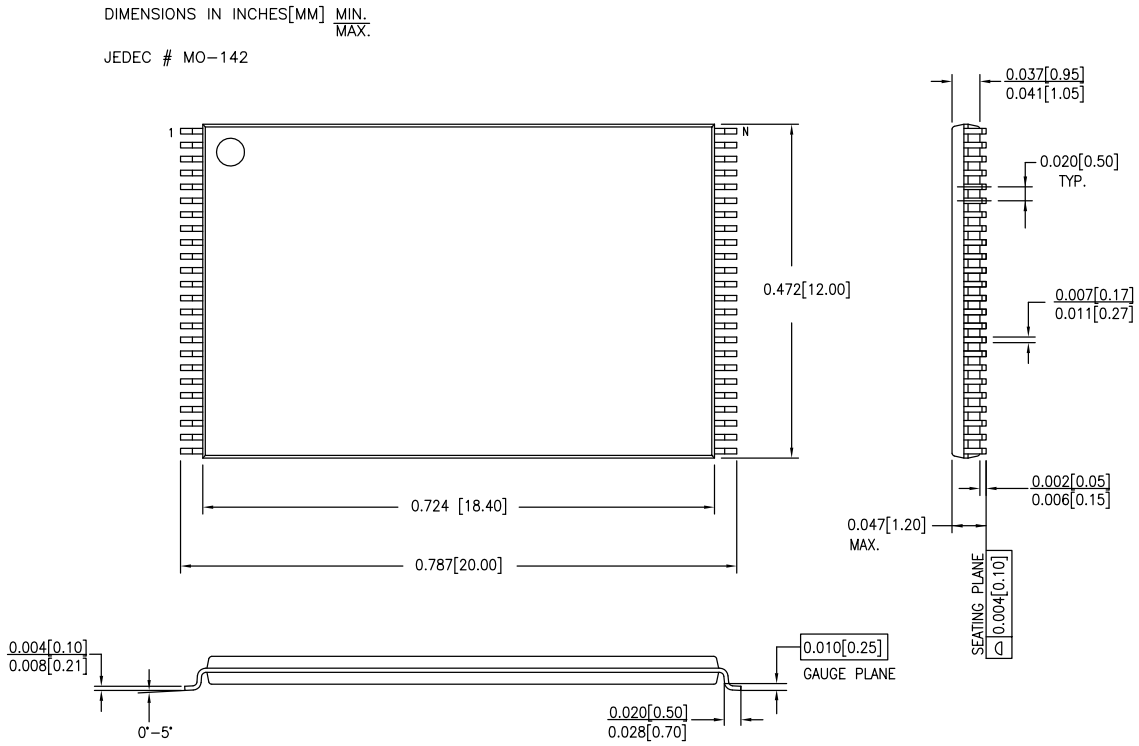
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	Operating Range
10	2.2 V–3.6 V	CY7C1061G30-10ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm)	Single Chip Enable without ERR	Industrial
		CY7C1061GE30-10ZXI			Single Chip Enable with ERR output at pin 6	
		CY7C1061G30-10ZSXI	51-85160	54-pin TSOP II (22.4 × 11.84 × 1.0 mm)	Dual Chip Enable without ERR	
		CY7C1061GE30-10ZSXI			Dual Chip Enable with ERR output at pin 43	
		CY7C1061G30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Dual Chip Enable without ERR Address MSB A_{19} at ball H6	
		CY7C1061GE30-10BVXI			Dual Chip Enable with ERR output at ball E3 Address MSB A_{19} at ball H6	
		CY7C1061G30-10BV1XI			Single Chip Enable without ERR Address MSB A_{19} at ball G2	
		CY7C1061G30-10BVJXI			Dual Chip Enable without ERR Address MSB A_{19} at ball G2	
15	1.65 V–2.2 V	CY7C1061G18-15BV1XI			Single Chip Enable without ERR Address MSB A_{19} at ball G2	Industrial

Ordering Code Definitions



Package Diagrams

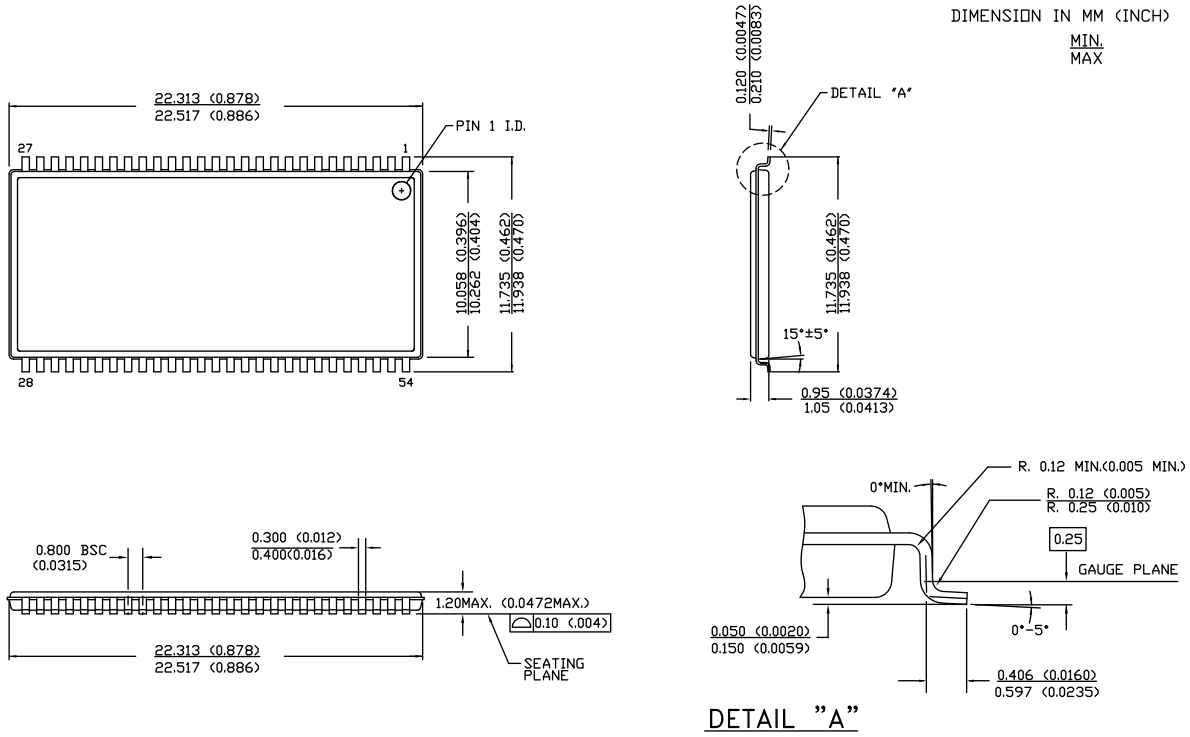
Figure 20. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183



51-85183 *C

Package Diagrams (continued)

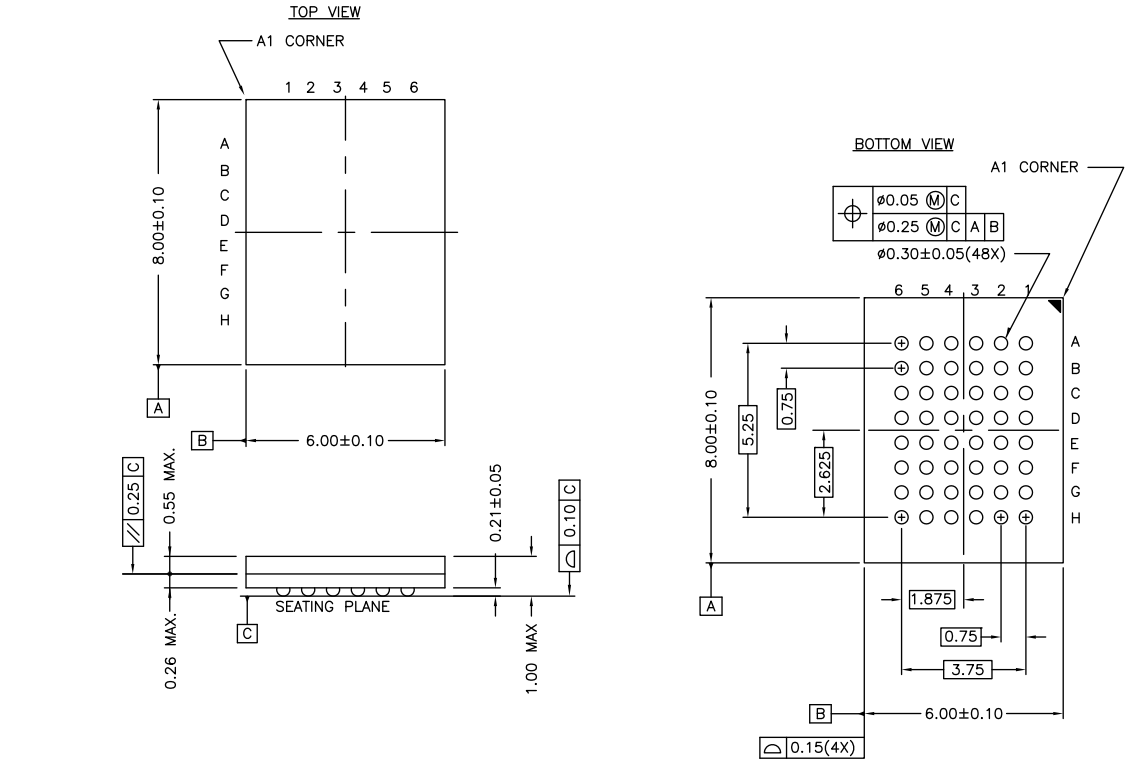
Figure 21. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 *E

Package Diagrams (continued)

Figure 22. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
$\overline{OE}$	Output Enable
SRAM	Static random access memory
TSOP	Thin small outline package
TTL	Transistor-transistor logic
VFBGA	Very fine-pitch ball grid array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This section describes the errata for the 16-Mbit asynchronous FAST SRAM - CY7C1061G30 and CY7C1061GE30 - in 65-nm process technology. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

If you have questions, contact your local Cypress Sales Representative or raise a technical support case at www.cypress.com/go/support.

Part Numbers Affected

Part Number	Device Characteristics
CY7C1061G30 (all packages and options)	16-Mbit FAST SRAM
CY7C1061GE30 (all packages and options)	16-Mbit FAST SRAM

FAST SRAM[44] Qualification Status

Product Status: All Engineering Samples (**Note:** Reliability qualification is not complete. These samples are recommended to be used only for engineering builds and evaluation, and not for production builds).

FAST SRAM[44] Errata Summary

This table defines the errata applicability to available 16-Mbit devices.

Items	Part Numbers	Silicon Rev	Fix Status
FAST SRAM[44] does not meet 10-ns speed -in AC switching parameters as specified in the datasheet specifications.	CY7C1061G30 CY7C1061GE30	*A	Fixed devices to be available from May 12, 2014.

■ Problem Definition

CY7C1061G30 and CY7C1061GE30 do not meet 10 ns speed in AC switching parameters as specified in Table 1.

■ Parameters Affected

AC switching parameters

■ Trigger Condition

Functionality is not guaranteed when the device is operated at speed of 10 ns.

■ Scope of Impact

This issue may not pose problems for most end systems because they may incorporate some margin to the datasheet specifications. The deviation from the datasheet specified limit of 10 ns is 2 ns.

■ Workaround

The RAM controller timing needs additional margin to accommodate the slower speed.

■ Fix Status

The fix for the above issue is in progress. Fixed devices will be available from May 12, 2014.

Note
44. This applies to all MPNs mentioned in Part Numbers Affected.

AC Switching Characteristics

Table 1. Comparison of AC Switching Parameters for 10 ns and 12 ns Parts

Parameter	Description	-10 ns		-12 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	12	–	ns
t_{AA}	Address to data valid	–	10	–	12	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ Low to data valid	–	10	–	12	ns
t_{DOE}	$\overline{OE}$ Low to data valid	–	5	–	7	ns
t_{LZOE}	$\overline{OE}$ Low to low-Z	1	–	1	–	ns
t_{HZOE}	$\overline{OE}$ High to high-Z	–	5	–	7	ns
t_{LZCE}	$\overline{CE}$ Low to low-Z	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ High to high-Z	–	5	–	7	ns
t_{PU}	$\overline{CE}$ Low to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ High to power-down	–	10	–	12	ns
t_{DBE}	Byte Enable to data valid	–	5	–	7	ns
t_{LZBE}	Byte Enable to low-Z	1	–	1	–	ns
t_{HZBE}	Byte Disable to high-Z	–	6	–	7	ns
Write Cycle						
t_{WC}	Write cycle time	10	–	12	–	ns
t_{SCE}	$\overline{CE}$ Low to write end	7	–	9	–	ns
t_{AW}	Address setup to write end	7	–	9	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	9	–	ns
t_{SD}	Data setup to write end	5	–	7	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ High to low-Z	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ Low to high-Z	–	5	–	7	ns
t_{BW}	Byte Enable to end of write	7	–	9	–	ns

Document History Page

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3690091	TAVA	07/27/2012	New data sheet.
*A	3776318	AJU	10/30/2012	Updated Document title to “CY7C1061G/CY7C1061GE, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)”. Updated Features (highlighted typical I_{CC}, included ECC feature). Updated Functional Description (Corrected typos, included 48-pin TSOP I information). Removed Selection Guide. Added 48-ball VFBGA pinouts (Figure 2, Figure 5, and Figure 6), added 48-pin TSOP I (Figure 7), and 54-pin TSOP II (Figure 10). Updated Product Portfolio to list all product options and added typical values for I_{CC} and I_{SB2} parameters. Changed latch up current limit from 200 to 140 mA (per JEDEC limits). Updated DC Electrical Characteristics: Changed maximum value of I_{CC} parameter from 100 mA to 110 mA for the Test Condition f = 100 MHz. Changed maximum value of I_{SB1} parameter from 30 mA to 40 mA. Changed maximum value of I_{SB2} parameter from 25 mA to 30 mA. Updated I_{SB2} test conditions to reflect correct CMOS input levels. Added Note 9 and referred the same note in Test Conditions of I_{SB1}, I_{SB2} parameters. Changed C_{IN} and C_{OUT} values for 54 TSOP and 48 BGA packages from 6/8 pF to 10 pF. Included 48-pin TSOP I information in Capacitance and Thermal Resistance. Updated Data Retention Characteristics Changed maximum value of I_{CCDR} parameter from 25 mA to 30 mA. Added Note 13 and referred the same note in Test Conditions of I_{CCDR} parameter and Figure 12. Updated AC Switching Characteristics: Removed redundant t_{POWER} parameter and associated footnote (captured in Note 12). Updated Note 16 to include difference in input levels for V_{CC} operation of less than 3 V. Added Note 18. Updated Note 22 for better clarity. Removed the Note “The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.” and its references.

Document History Page (continued)

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A (cont.)	3776318	AJU	10/30/2012	Updated Switching Waveforms: Updated Note 24 for better clarity. Updated Figure 15 to make it applicable to both CY7C1061G and CY7C1061GE. Updated Note 26 for better clarity. Updated Note 28 to correct typos. Referred Notes 29 and 30 in Figure 16 and Figure 17. Referred Notes 38 and 39 in Figure 19. Updated Notes 31 and 40 for better clarity. Removed the Note "If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state." and its references (captured in Note 31 and Note 40). Updated Truth Table (Referred Note 42 in $\overline{CE}$ column and added footnote 33). Updated Ordering Information. Updated Package Diagrams with the updated revisions.
*B	4003550	AJU	05/17/2013	No technical updates.
*C	4042263	AJU	06/27/2013	Updated Data Retention Characteristics: Changed minimum value of V_{DR} parameter from 1.5 V to 1 V. Updated AC Switching Characteristics: Changed maximum value of t_{HZBE} parameter from 5 ns to 6 ns for 10 ns speed bin. Changed minimum value of t_{SD} parameter from 5.5 ns to 5 ns for 10 ns speed bin.
*D	4120023	MEMJ	09/11/2013	Updated Features: Changed typical value of I_{SB2} from 10 mA to 20 mA. Replaced "1.5-V data retention" with "1.0 V data retention". Updated Data Retention Waveform: Changed value of V_{DR} from 1.5 V to 1 V. Updated AC Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 1 ns to 0 ns for 10 ns speed bin. Changed minimum value of t_{LZBE} parameter from 1 ns to 0 ns for 10 ns speed bin. Updated Ordering Information (Updated part numbers). Added Errata. Updated in new template.

Document History Page (continued)

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	4163557	MEMJ	10/29/2013	Updated Pin Configurations: Added Figure 3. Updated DC Electrical Characteristics: Added minimum value of I_{SB2} parameter. Added Note 10 and referred the same note in minimum value of I_{SB2} parameter. Updated Ordering Information: Updated part numbers. Updated details in “Key Features / Differentiators” column corresponding to MPN “CY7C1061GE30-10BVXI” (Corrected ERR output location from ball G2 to ball E3).
*F	4272659	MEMJ	02/05/2014	Updated AC Switching Characteristics: Added Note 20 and referred the same note in description of t_{LZOE}, t_{HZOE}, t_{LZCE}, t_{HZCE}, t_{LZBE}, t_{HZBE}, t_{LZWE}, t_{HZWE} parameters.
*G	4292074	MEMJ / VINI	03/07/2014	Updated Features section Introduced 15-ns speed bin Mentioned frequency for I_{CC} typical measurement Changed "an error detection" to "a single-bit error detection" Updated DC Electrical Characteristics: Added column for Typical values Moved reference to Note 10 from I_{SB2} (Typical) to the "Typ" column heading Updated AC Switching Characteristics: Added t_{POWER} and associated Note 17. Added Note 23 and referred to Write Cycle timings Referred Note 19 to t_{HZBE} and t_{LZBE} Added Note 32 in Figure 17. Added Figure 18 ($\overline{WE}$ controlled write) Added Note 33 in Figure 16 and Figure 17, Note 37 in Figure 18, and Note 41 in Figure 19 to indicate output state. Added condition to place outputs in disable state by making both $\overline{BHE}$ and $\overline{BLE}$ HIGH in Truth Table. Corrected ERR table by replacing “no error in stored data” with “no single bit error in stored data” Clarified different ordering options with respect to with or without ERR, location of ERR, and address MSB A_{19} in Ordering Information. Updated Errata Fix status
*H	4330547	AJU	04/02/2014	No content update.
*I	4375287	AJU	05/09/2014	Updated Errata: Updated FAST SRAM[44] Errata Summary: Updated date in “Fix Status” column in table and also “Fix Status” in bulleted points below the table. Completing Sunset Review.
*J	4397546	VINI	06/03/2014	Updated footnote 19 - removed tLZOE, tLZCE, tLZWE, and tLZBE, and added Hi-Z, Lo-Z transition.
*K	4469360	NILE	09/18/2014	Updated Package Diagrams: spec 51-85160 – Changed revision from *D to *E.

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